WHAT IS CLAIMED IS:

1. A programmable clock generator for providing multiple clock signals with non-overlapping edges, comprising:

means for receiving an external signal from an external clock and providing first and second clock signals as a result of said external signal;

first programmable delay means, coupled to said receiving means, for delaying said first clock signal and feeding a resultant delayed first clock signal back into said receiving means to change the phase of said second clock signal based on the amount of delay introduced by said first programmable delay means; and

second programmable delay means coupled to said receiving means, for delaying said second clock signal and feeding a resultant delayed second clock signal back into said receiving means to change the phase of said first clock signal based on the amount of delay introduced by said second programmable delay means.

2. The programmable clock generator of claim 1, wherein said means for receiving comprises:

a first logic gate, having first and second input terminals and a first output terminal, said first input terminal coupled to the said external clock for receiving said external clock signal, wherein said first output terminal produces said first clock signal;

a second logic gate, having third and fourth input terminals and a second output terminal, said fourth input terminal having an inverter coupled to said external clock for inverting said external clock signal, wherein said output terminal of said second logic gate produces said second clock signal.

3. The programmable clock generator of claim 1, wherein said first and second programmable delay means each comprise:

a plurality of delay elements connected in series to form a delay path; and

means for altering the number of delay elements comprising said delay.

4. The programmable clock generator according to claim 3, wherein said means for altering comprises:

a conductive path having a switch, said conductive path connected in parallel with a delay element in said delay path, operable to short out said delay when said switch is closed.

5. The programmable clock generator according to claim 3, wherein said means for altering comprises:

a plurality of connection points at different locations along said delay path; and

a programmable switch for receiving a delayed clock signal from each of said connection points and selecting one of said delayed clock signals.

6. The programmable clock generator according to claim 1, wherein said first and second programmable delay means each comprise:

a plurality of delay paths each having a different delay time; and

means for selecting one of said delay paths.

7. A programmable clock generator for receiving a single clock signal and for providing multiple clock signals having non-overlapping clock edges with adjustable distances between said non-overlapping clock edges, comprising:

a first logic gate, having a first and second input terminals and a first output terminal, said first input terminal coupled to the single clock signal

for receiving the single clock signal, wherein said first output terminal produces a first clock signal having edges;

a second logic gate, having third and fourth input terminals and a second output terminal, said fourth input terminal having an inverter coupled to the single clock signal for inverting the single clock signal, wherein said output terminal of said second logic gate produces a second clock signal having edges;

a first programmable delay path, coupled between said first output terminal and said third input terminal, for controlling distances between said clock edges of said first and second clock signals; and

a second programmable delay path, coupled between said second output terminal of said second logic gate and said second input terminal of said first logic gate, for controlling distances between said clock edges of said first and second clock signals.

8. The programmable clock generator of claim 7, wherein said firs programmable delay path comprises:

a first conductive path comprising delay elements for delaying said first clock signal, said first conductive path having an input node and an output node; and

a second conductive path coupled to said input and output nodes in parallel to said delay elements, said second conductive path having a first switch whereby said first clock signal bypasses said first conductive path via said second conductive path when said first switch is closed and said input node and said output node are shorted together.

9. The programmable clock generator of claim 8, wherein said first conductive path further comprises a second switch coupled to said output node and said delay elements operable to be opened when said first switch is closed.

10. The programmable clock generator of claim 7, wherein said second programmable delay path comprises:

a first conductive path comprising delay elements for delaying said second clock signal, said first conductive path having an input node and an output node; and

a second conductive path coupled to said input and output nodes in parallel to said delay elements, said second conductive path having a first switch whereby said second clock signal bypasses said first conductive path via said second conductive path, when said first switch is closed and said input node and said output node are shortened together.

11. The programmable clock generator of claim 10, wherein said second conductive path further comprises a second switch coupled to said output node and said delay elements operable to be opened when said first switch is closed.

12. A method of generating non-overlapping clocks, comprising the steps of:

(a) receiving an external clock signal and inverting said external clock signal to provide an inverted clock signal;

(b) generating a first clock signal and a second clock signal based on said external clock signal and aid inverted external clock signal, respectively;

(c) delaying said first clock signal by an adjustable amount of delay to provide a delayed first clock signal and using said delayed first clock signal to alter the phase of said second clock signal;

(d) delaying said second clock signal by an adjustable amount of delay to provide a delayed second clock signal and using said delayed second clock signal to alter the phase of said first clock signal; and

(e) adjusting said amount of delay introduced in steps (c) and (d) to optimize edge placement of said first and second clock signals.

13. The method of claim 12, wherein said step (c) comprises the step of routing said first clock signal through a first delay path comprising a plurality of discrete delay elements.

14. The method of claim 12, wherein said step (d) comprises the step of routing said second clock signal through a second delay path comprising a plurality of discrete delay elements.

15. The method of claim 12, wherein said step (e) comprises the step of shunting at a delay element to bypass said delay element and thereby alter the number of delay elements in at least one of said first and second delay paths.

16. The method of claim 12, wherein said step (c) comprises the step of routing said first clock signal through a first delay path comprising a plurality of discrete delay elements and first connection points.

17. The method of claim 12, wherein said step (d) comprises the step of routing said second clock signal through a second delay path comprising a plurality of discrete delay elements and second connection points.

18. The method of claim 12, wherein said step (e) comprises the step of selecting said first and second delayed clock signal from among said plurality of first and second connection points, respectively.

19. The method of claim 12, wherein said step (e) comprises the steps of:

selecting a first delay path from a first plurality of delay paths of varying length;

routing said first clock signal through said first delay path to provide said delayed first clock signal;

selecting a second delay path from a second plurality of delay paths of varying length; and

routing said second clock signal through said second delay path to provide said delayed second clock signal.